of output data,

the method comprising, for a set of input data and a set of output data, the following steps:

a configuration step in which the memory system is set up by means of control commands associated with the set of input data and the set of output data; and

an execution step in which, on the basis of the control commands, the memory system:

ensures that input data and output data are not simultaneously required for writing and reading from one of the plurality of memory circuits.

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REMARKS

Claims 1-5 remain pending in this application. Claims 1, 4 and 5, the independent claims, have been amended. Favorable reconsideration is respectfully requested.

In the Office Action, Claims 1-5 were rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way to convey that Applicant had possession of the claimed invention.

Applicant submits that support for the features noted in the Office Action can at least be found at page 4, lines 21-25. Withdrawal of the Section 112 rejection is respectfully requested.

Claims 1-5 were also rejected under 35 U.S.C. ɔ 102 as being anticipated by U.S. Patent 4,734,850 (Torii et al.)

Applicant respectfully submits that the rejected claims as amended are patentable for at least the following reasons.

Claim 1 as amended is directed to a data processing arrangement including a first processor for providing successive sets of input data, a second processor for receiving successive sets of output data and a memory system including a plurality of memory circuits where each of the plurality of memory circuits is accessible by the first processor and the second processor. A master controller for setting up the plurality of independent memory circuits of the memory system using control commands associated with a set of input data and a set of output data and a control unit for, on the basis of the control commands, ensuring that input data and output data are not simultaneously required for writing and reading from one of the plurality of memory circuits are also included.

As understood by Applicant, Torii et al. relates to a data process system that includes plural storage means each one of which is capable of concurrent and intermediate reading and writing of a set of data signals. As shown in Fig. 1, while multiple FIFO memory units (20-22) are shown, only one respective E-unit (4-6) is capable of accessing any one of the FIFO memory units. In contrast, as shown the embodiment of Fig. 1 of the present invention, each memory unit (MEM1-5) is accessible by both processors (PROC1 and 2).

It is also noted that in Fig. 7 of the Torii et al. the FIFO memories are allocated to input or output ports using the distribution logic circuit 911 (col. 16, lines 2-9) and are not all accessible by the E-units (901-903).

Nothing has been found in Torii et al., however that teaches a control unit for, on the basis of the control commands, ensuring that input data and output data are not simultaneously required for writing and reading from one of the plurality of memory circuits

and where the each of the plurality of memory circuits is accessible by a first and a second processor, as recited in Claim 1.

The Office Action states that Torii et al. teaches an arrangement that ensures that input data and output data are not simultaneously required for writing and reading from the same memory. However, it is noted that Torii et al. specifically teaches that a "selected FIFO memory performs read and write operations concurrently and intermittently." (See Abstract; see also col. 1, lines 36-38, and col. 2, lines 58-60).

At least for the above reasons, Claim 1 is believed patentable over Torii et al.

Independent Claims 4 and 5 recite similar features as recited in Claim 1, and are believed allowable for at least the same reason.

A review of the other art of record has failed to reveal anything which, in Applicant's opinion, would remedy the deficiencies of the art discussed above, as reference a against the independent claims. Those claims are therefore believed patentable over the art of record.

The other rejected claims in this application are each dependent from one or another of the independent claims discussed above and are therefore believed patentable for the same reasons. In addition, however, each dependent claim is also deemed to define an additional aspect of the invention, and should be individually considered on its own merits.

This Amendment After Final Rejection is believed clearly to place this application in condition for allowance and its entry is therefore believed proper under 37 C.F.R. § 1.116. In any event, however, entry of this Amendment After Final Rejection, as an earnest effort to advance prosecution and reduce the number of issues, is respectfully requested.

In view of the foregoing amendments and remarks, Applicant respectfully requests favorable reconsideration and early passage to issue of the present application.

Applicant's undersigned attorney may be reached by telephone at the number given below.

Respectfully submitted,

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On August 29, 2002

By _____
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## Appendix of Marked-up Claims

1. (Amended) A data processing arrangement comprising:

a first processor for providing successive sets of input data;

a second processor for receiving successive sets of output data;

a memory system ~~comprising~~ including a plurality of ~~independent~~ memory circuits ~~shared~~where each of the plurality of memory circuits is accessible by the first processor and the second processor ~~for receiving the successive sets of input data and providing the successive sets of output data~~;

a master controller for setting up the plurality of independent memory circuits of said memory system using control commands associated with a set of input data and a set of output data; and

a control unit for, on the basis of the control commands, ensuring that input data and output data are not simultaneously required for writing and reading from one of the plurality of ~~independent~~ memory circuits.

4. (Amended) A memory system comprising:

a plurality of ~~independent~~ memory circuits for receiving successive sets of input data and for providing successive sets of output data, the plurality of memory circuits being accessible by at least two processors;

a control unit being programmable by means of control commands associated with a set of input data and a set of output data and, on the basis of these control commands, for ensuring that input data and output data are not simultaneously required for writing and reading from one of the plurality of ~~independent~~ memory circuits.

5. (Amended) A method of processing data in a data processing arrangement including a first processor for providing successive sets of input data, a second processor for receiving successive sets of output data and a memory system including a plurality of ~~independent~~ memory circuits that are accessible ~~shared~~ by both the first and processor and the second processor for receiving the successive sets of input data and providing the successive sets of output data,

the method comprising, for a set of input data and a set of output data, the following steps:

a configuration step in which the memory system is set up by means of control commands associated with the set of input data and the set of output data; and

an execution step in which, on the basis of the control commands, the memory system:

ensures that input data and output data are not simultaneously required for writing and reading from one of the plurality of ~~independent~~ memory circuits.